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| **VELS INSTITUTE OF SCIENCE, TECHNOLOGY AND ADVANCED STUDIES (VISTAS)**  **COURSE/LESSON PLAN** |
| **Faculty Name**: Dr.A.Banushri **Designation**: Assistant Professor **Dept**:CSE  **Course Name/Course Code:**COMPUTER ORGANIZATION AND ARCHITECTURE / 21CBDS42 |
| **Class/Year/Sem: B.Tech DS/II A/IV** |

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| **S.No** | **Period** | **Topics to be covered** | **Date** | | **Text/Reference Book**  **Name/No** | **Teaching Aids**  (PPT / OHP/ BOARD/ CHART/ MODEL/  A-V/ EDUTECH/ EDUSAT) | **Initial of Staff** | **Initial of HOD** |
| **Proposed** | **Actual** |
| **UNIT I PHYSICAL LAYER AND MEDIA** | | | | | | | | |
| **1** |  | Functional units, Basic operational concepts, Bus structures |  |  | T1 – Ch 1; Pg 1-5 | BOARD |  |  |
| **2** |  | Performance and metrics, Instructions and  instruction sequencing |  |  | T1 – Ch 1; Pg 6-11 | BOARD |  |  |
| **3** |  | Hardware Software Interface |  |  | T1 – Ch 1; Pg 12-24 | BOARD |  |  |
| **4** |  | Instruction set architecture |  |  | T1 – Ch 2; Pg 32-41 | BOARD |  |  |
| **5** |  | Addressing modes |  |  | T1 – Ch 2; Pg 41-49 | BOARD |  |  |
| **6** |  | RISC – CISC |  |  | T1 – Ch 3; Pg 80-108 | BOARD |  |  |
| **7** |  | ALU design |  |  | T1 – Ch 1; Pg 1-5 | BOARD |  |  |
| **8** |  | Fixed point and floating point operations |  |  | T1 – Ch 1; Pg 6-8 | BOARD |  |  |
| **9** |  | Floating Point Numbers and Operations. |  |  | T1 – Ch 1; Pg 8-20 | BOARD |  |  |
| **UNIT II BASIC PROCESSING UNIT** | | | | | | | |  |
| **1** |  | Some Fundamental concepts |  |  | T1 – Ch 10; Pg 211-222 | PPT |  |  |
| **2** |  | Execution of a complete instruction: Branch instructions |  |  | T1 – Ch 11; Pg 241-243 | PPT |  |  |
| **3** |  | Multiple bus  organization |  |  | T1– Ch 11; Pg 244-246 | PPT |  |  |
| **4** |  | Hardwired control: A Complete Processor |  |  | T1 – Ch 11; Pg 247-249 | PPT |  |  |
| **5** |  | Micro programmed control: Microinstructions |  |  | T1 – Ch 11; Pg 250-258 | PPT |  |  |
| **6** |  | Microprogram Sequencing – Wide-Branch Addressing |  |  | T1 – Ch 12; Pg 264-265 | PPT |  |  |
| **7** |  | Microinstructions with next address field |  |  | T1 – Ch 12; Pg 265-268 | PPT |  |  |
| **8** |  | Prefetching  and emulation |  |  | T1 – Ch 12; Pg 269-272 | PPT |  |  |
| **9** |  | Nano programming |  |  | T1 – Ch 12; Pg 273-279 | PPT |  |  |
|  | | | | | | | |  |
| **1** |  | Basic concepts: Role of Cache Memory |  |  | T1 – Ch 2; Pg 23-27 | BOARD |  |  |
| **2** |  | Pipeline Performance – Data Hazards |  |  | T1 – Ch 2; Pg 28-31 | BOARD |  |  |
| **3** |  | Instruction Hazards – Influence  on Instruction Sets: Addressing modes |  |  | T1 – Ch 3; Pg 35-39 | BOARD |  |  |
| **4** |  | Condition Codes – Datapath and Control Considerations |  |  | T1 – Ch 3; Pg 43-50 | BOARD |  |  |
| **5** |  | Superscalar  Operation |  |  | T1 – Ch 4; Pg 55-61 | BOARD |  |  |
| **6** |  | Dispatch Operation |  |  | T1 – Ch 4; Pg 62-66 | BOARD |  |  |
| **7** |  | Out-of-Order Execution Execution Completion |  |  | T1 – Ch 5; Pg 71-83 | BOARD |  |  |
| **8** |  | Performance Considerations |  |  | T1 – Ch 5; Pg 91-99 | BOARD |  |  |
| **9** |  | Exception Handling |  |  | T1 – Ch 5; Pg 100-108 | BOARD |  |  |
| **10** |  | **Vels Enrichment**Programme - 1 |  |  |  | BOARD |  |  |
| **UNIT IV MEMORY SYSTEM** | | | | | | | |  |
| **1** |  | Basic concepts – Semiconductor RAM – ROM – Speed – Size and cost |  |  | T1 – Ch 7; Pg 111-122 | BOARD |  |  |
| **2** |  | Cache Memories: Mapping Functions |  |  | T1 – Ch 7; Pg 121-127 | BOARD |  |  |
| **3** |  | Replacement Algorithms Example |  |  | T1 – Ch 8; Pg 131-141 | BOARD |  |  |
| **4** |  | Performance Considerations: Interleaving |  |  | T1 – Ch 9; Pg 151-171 | BOARD |  |  |
| **5** |  | Hit Rate and Miss Penalty–  Caches on the Processor Chip |  |  | T1 – Ch 9; Pg 172-182 | BOARD |  |  |
| **6** |  | Virtual Memories |  |  | T1 – Ch 17; Pg 379-392 | BOARD |  |  |
| **7** |  | Memory Management Requirements |  |  | T1 – Ch 19; Pg 423-428 | BOARD |  |  |
| **8** |  | Associative Memories |  |  | T1 – Ch 19; Pg 423-428 | BOARD |  |  |
| **9** |  | Secondary Storage devices |  |  | T1 – Ch 19; Pg 429-439 | BOARD |  |  |
| **UNIT V I/O ORGANIZATION** | | | | | | | |  |
| **1** |  | Accessing I/O devices |  |  | T1 – Ch 18; Pg 395-412 | PPT |  |  |
| **2** |  | Interrupts : Interrupt Hardware Enabling and Disabling Interrupts |  |  | T1 – Ch 18; Pg 413-420 | PPT |  |  |
| **3** |  | Handling  Multiple Devices |  |  | T1 – Ch 20; Pg 441-448 | PPT |  |  |
| **4** |  | Controlling Device Requests |  |  | T1 – Ch 20; Pg 448-453 | PPT |  |  |
| **5** |  | Exceptions – Direct Memory Access: |  |  | T1 – Ch 10; Pg 185-209 | PPT |  |  |
| **6** |  | Bus Arbitration |  |  | T1 – Ch 11; Pg 213-242 | PPT |  |  |
| **7** |  | Buses:  Synchronous Bus Asynchronous Bus |  |  | T1 – Ch 12; Pg 247-252 | PPT |  |  |
| **8** |  | Interface circuits: Parallel Port Serial Port |  |  | T1 – Ch 13; Pg 277-293 | PPT |  |  |
| **9** |  | Standard I/O Interfaces  (PCI, SCSI, and USB), I/O devices and processors |  |  | T1 – Ch 14; Pg 307-323 | PPT |  |  |
| **10** |  | **Vels Enrichment**Programme - 2 |  |  |  | PPT |  |  |

**Text book:**

**T1**. Carl Hamacher, ZvonkoVranesic and SafwatZaky, “Computer Organization”, sixth Edition, Tata

McGraw Hill, 2011

**Reference Books**:

**R1.** William Stallings, “Computer Organization and Architecture – Designing for Performance”, eleventh Edition, Pearson Education, 2019.

**R2.** David A. Patterson and John L. Hennessy, “Computer Organization and Design: The Hardware/Software interface”,fifth Edition, Elsevier, 2014

**R3.** John P. Hayes, “and Organization”, Third Edition, Tata McGraw Hill, Computer Architecture 2012

**R4.** M. Morris Mano, “Computer system Architecture”, Third edition, Prentice Hall of India, 201**7**

**Journal / Weblink**

Link1:https://nptel.ac.in/courses/106105163

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